

U.S. PAT. 3,400,000

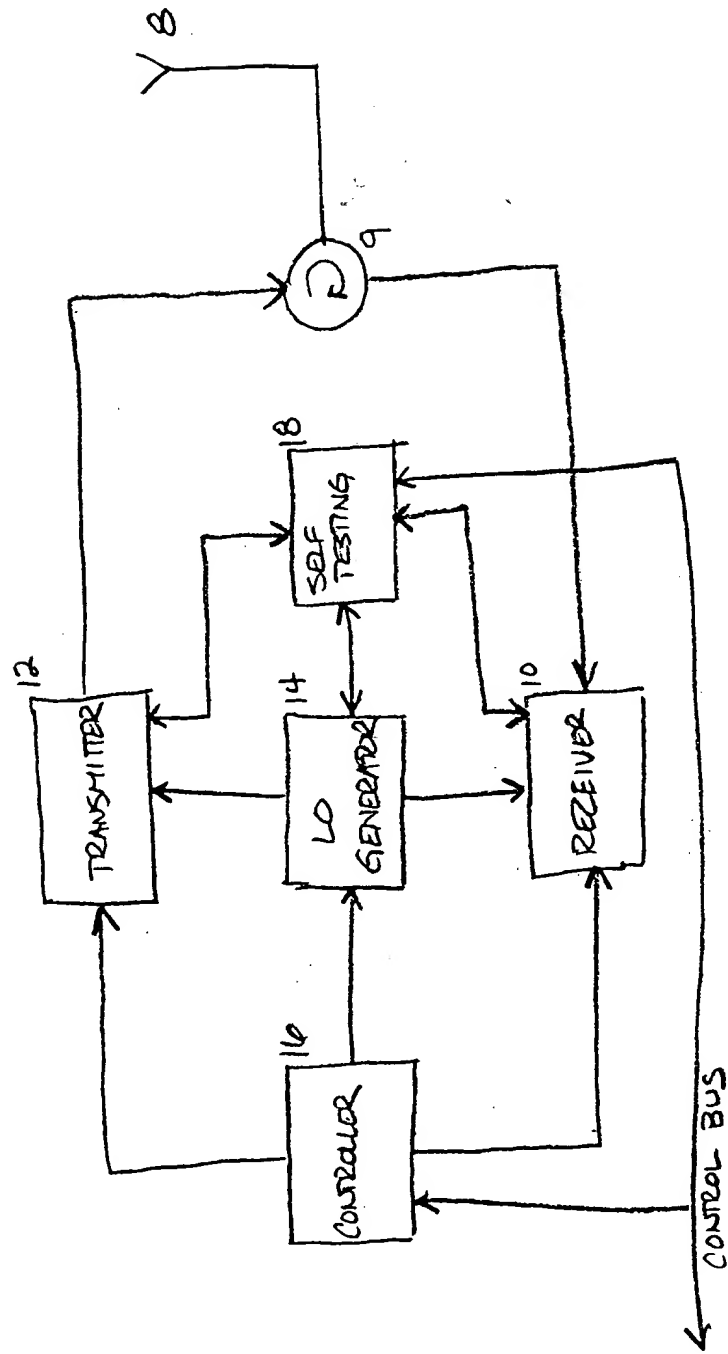


FIG. 1

The diagram illustrates a software-defined radio receiver architecture, divided into several functional blocks and sections:

- RF Front-End (Block 22):** Receives RF input and passes it through an LNA (Low Noise Amplifier) and a Select switch. A clock signal is provided to the LNA.
- Baseband Processor (Block 30):** Contains four mixers (represented by circles with an 'X') and a Programmable Gain Amplifier (PGA). It receives a clock signal and outputs I and Q signals.
- Baseband Processor (Block 32):** Contains a Discrete-Time Filter (DTF) and a Low-Pass Filter (LPF). It receives the I and Q signals and outputs Baseband signals.
- Baseband Processor (Block 36):** Contains a Demodulator and an A/D (Analog-to-Digital) converter. It receives the Baseband signals and outputs a Program signal.
- Calibration Section (Block 14):** Contains a Clock Generator (CLK GEN), a Divider, a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 40):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 42):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 44):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 46):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 48):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 50):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 52):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 54):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 56):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 58):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 60):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 62):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 64):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 66):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 68):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 70):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 72):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 74):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 76):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 78):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 80):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 82):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 84):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 86):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 88):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 90):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 92):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 94):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 96):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 98):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.
- Baseband Processor (Block 100):** Contains a PLL (Phase-Locked Loop), a Divider, and a Crystal Oscillator. It receives a Select signal and outputs a Program signal.

Fig. 2

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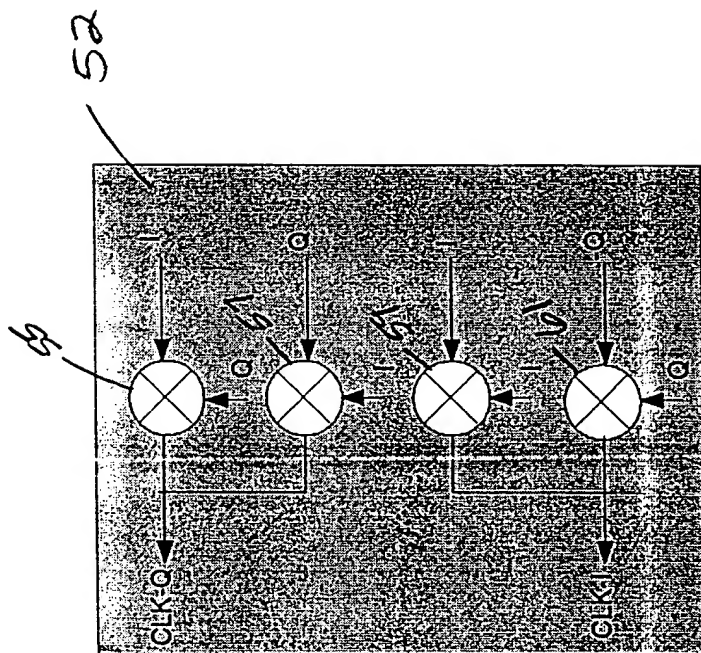


FIG. 3

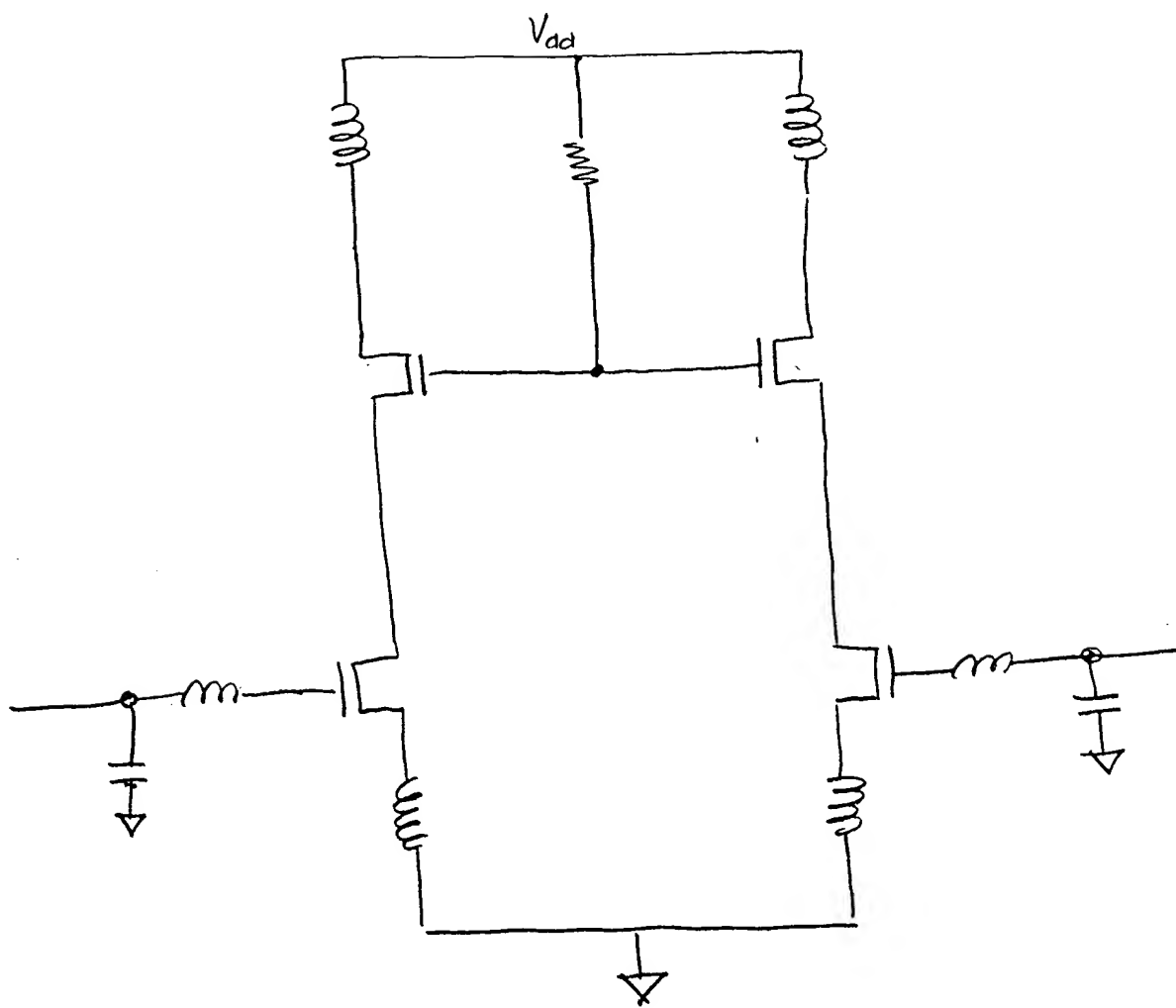


FIG. 4(a)

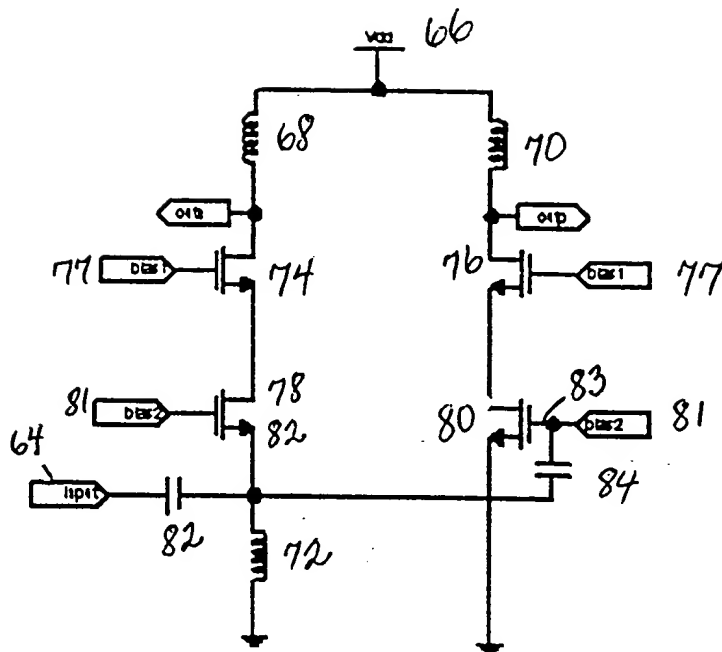


FIG. 4

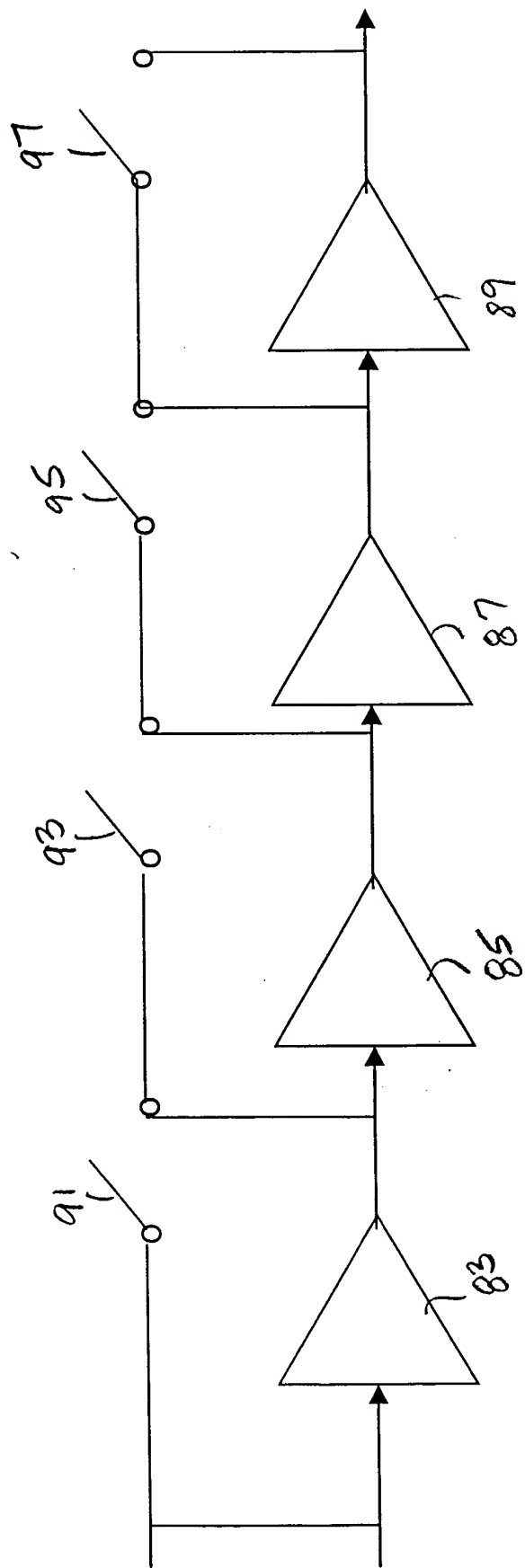


FIG. 5



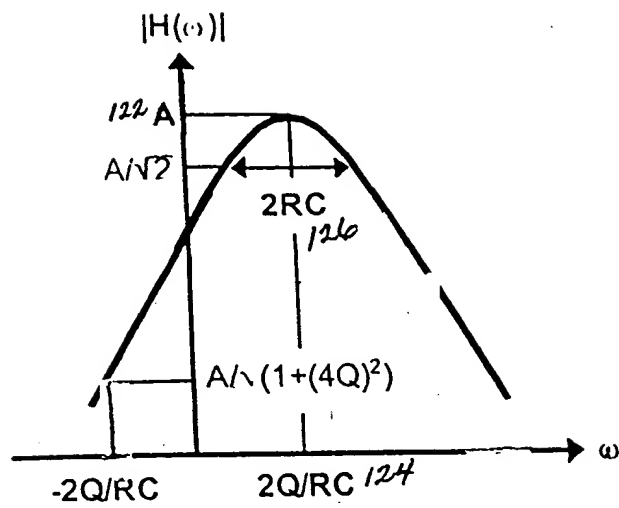


FIG. 7



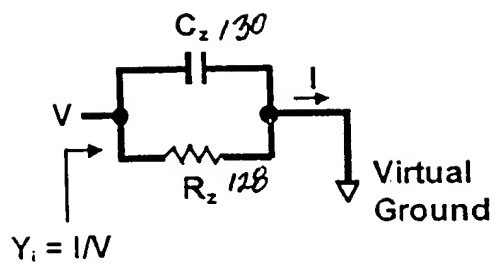


FIG. 8

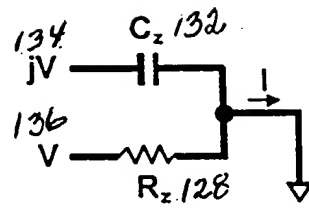


FIG. 9



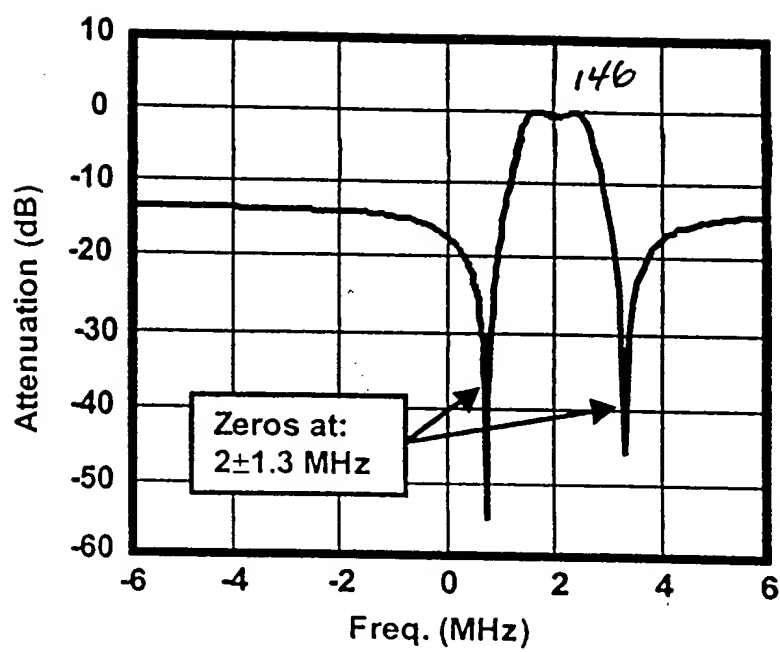


FIG. 11

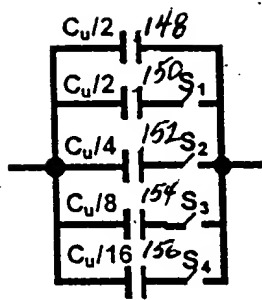


FIG. 12(a)

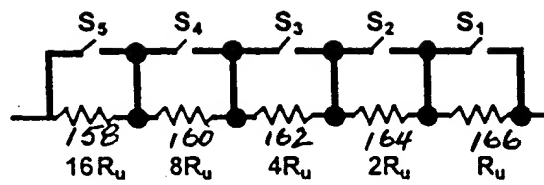


FIG. 12(b)

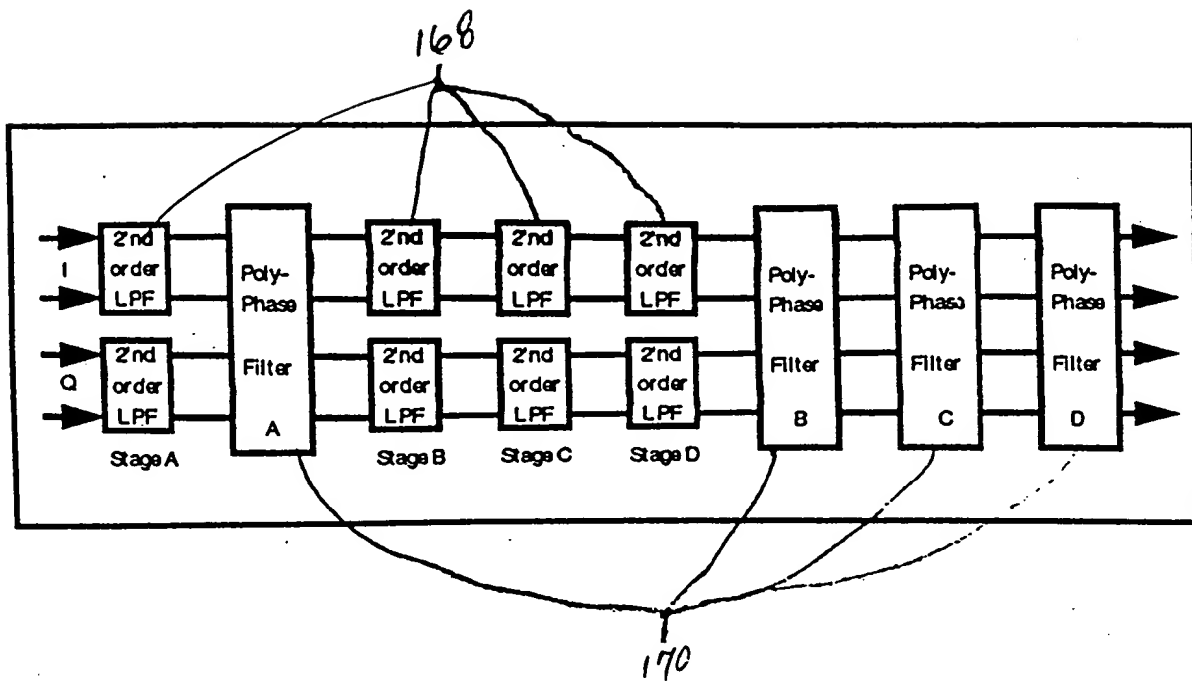


FIG. 13

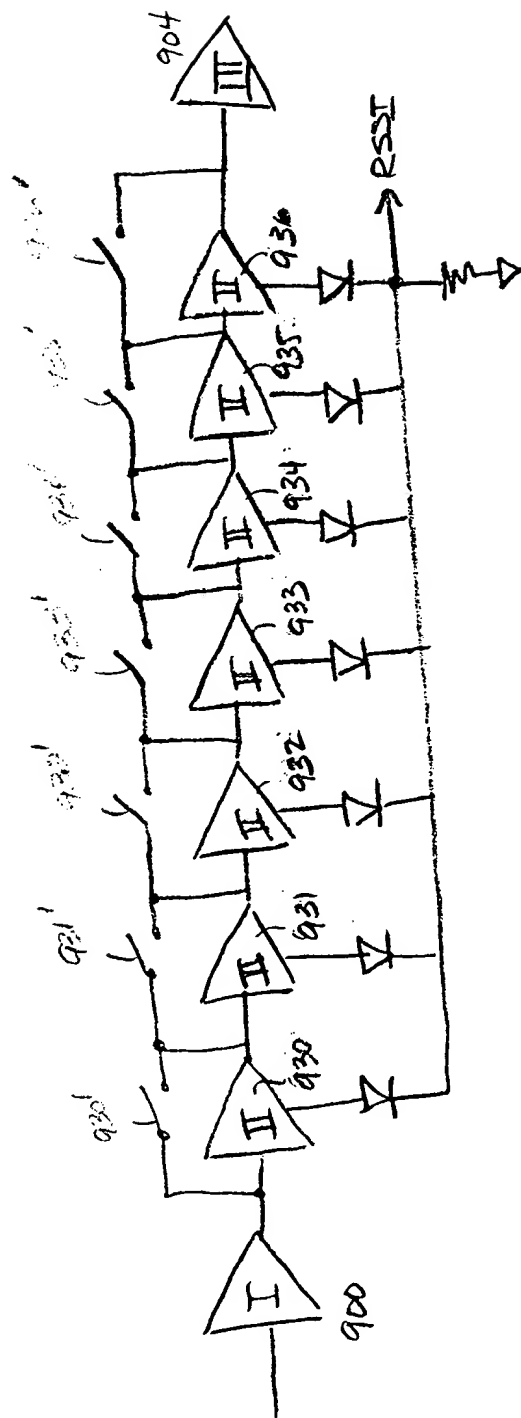


FIG. 14

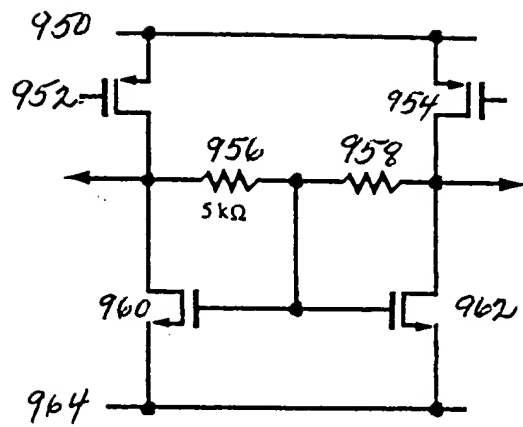


FIG. 15





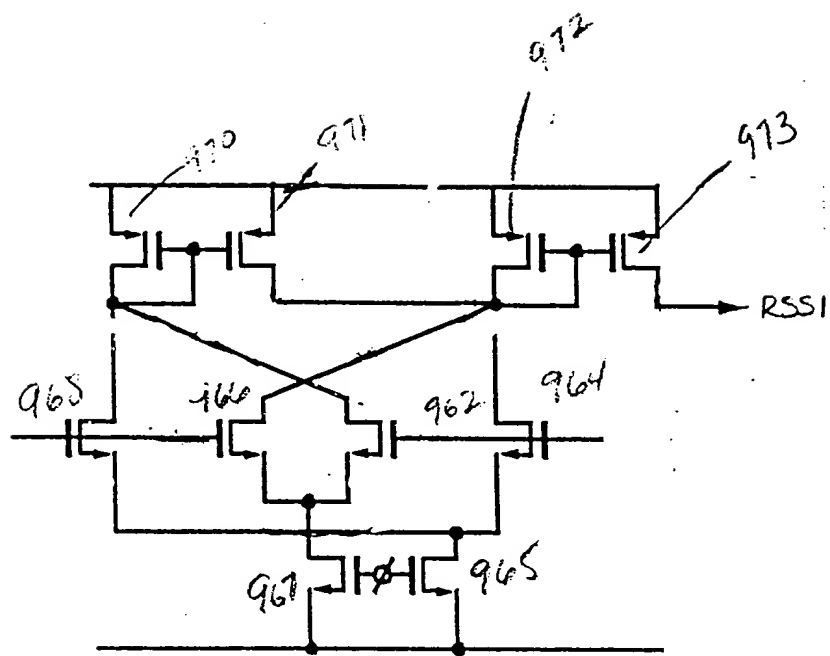


FIG. 17(a)

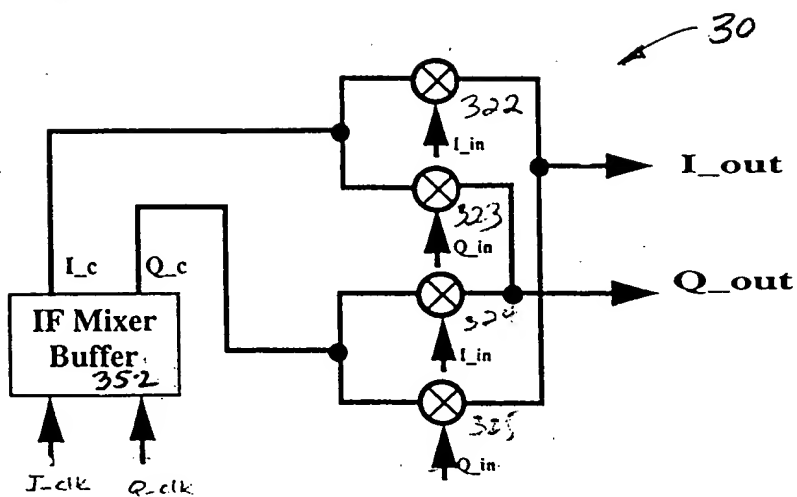


FIG. 17(b)

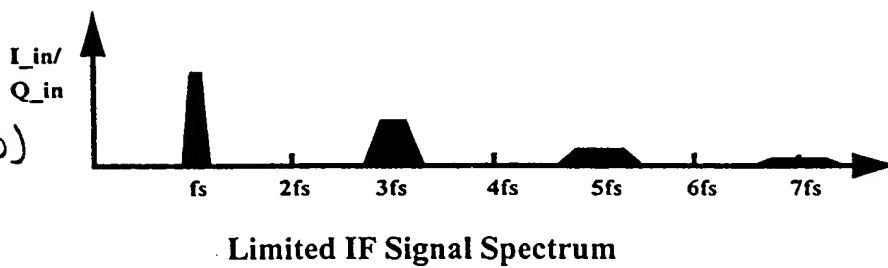


FIG. 17(c)

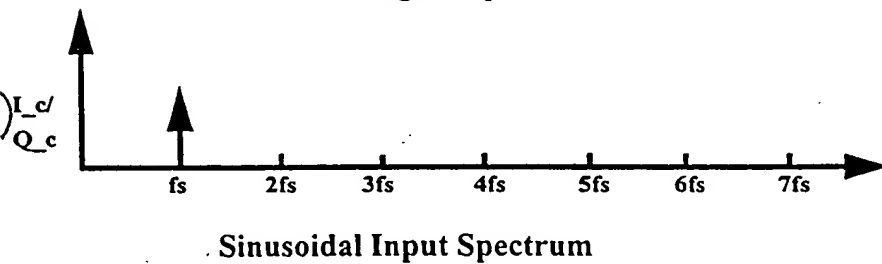


FIG. 17(d)

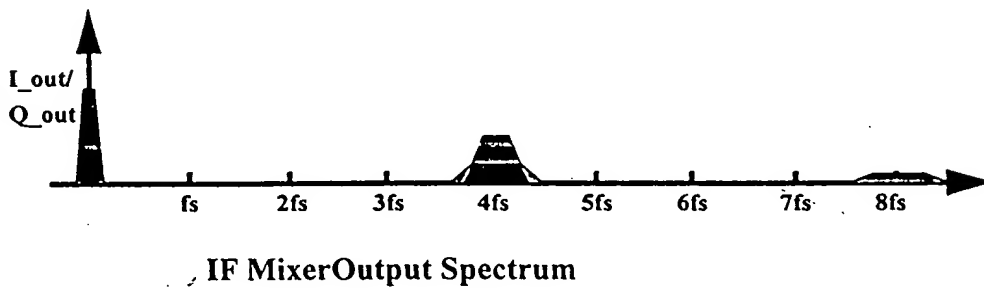


FIG. 18

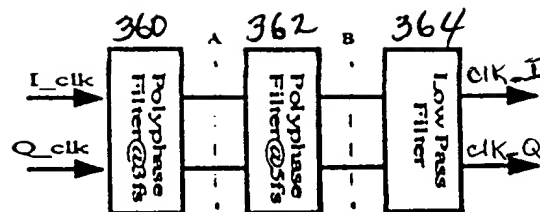


FIG. 19(a)

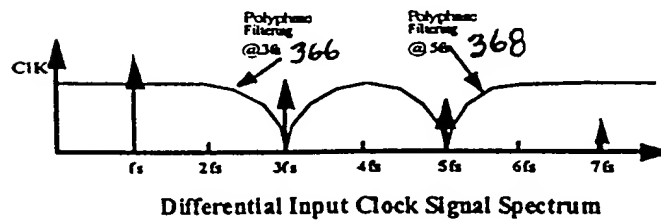


FIG. 19(b)

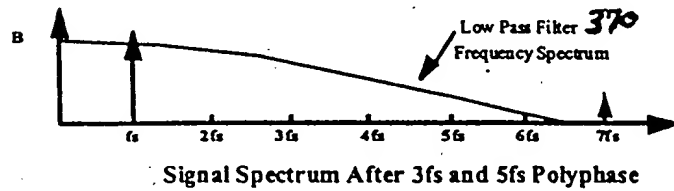
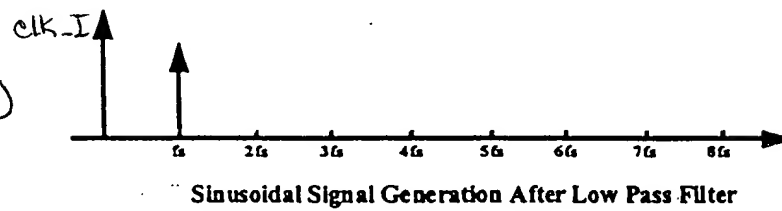
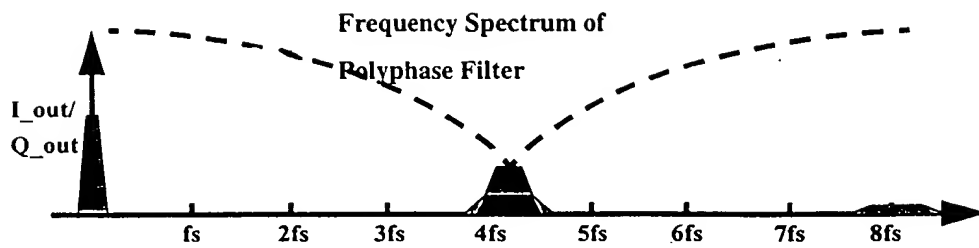


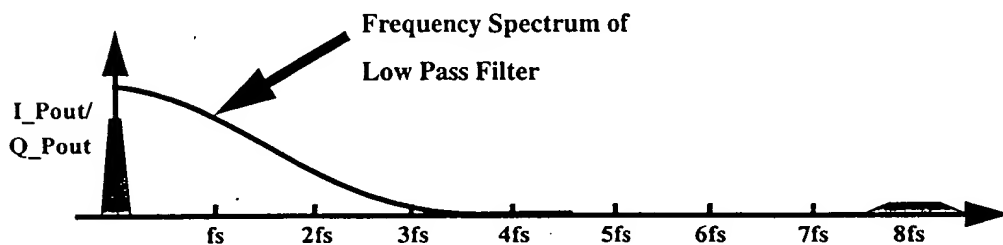
FIG. 19(c)





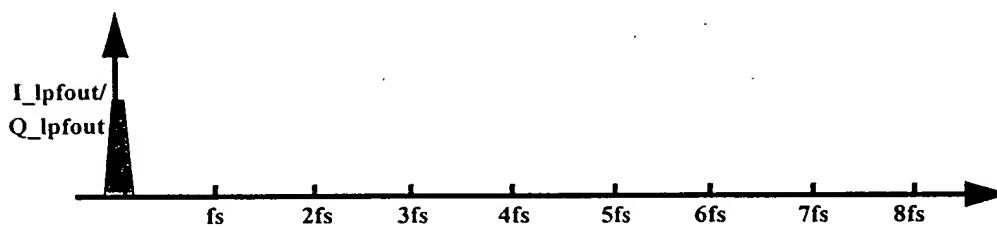
Signal Spectrum at Polyphase Input

FIG. 20(a)



Signal Spectrum at Polyphase Output

FIG. 20(b)



Signal Spectrum at Low Pass Filter Output

FIG. 20(c)

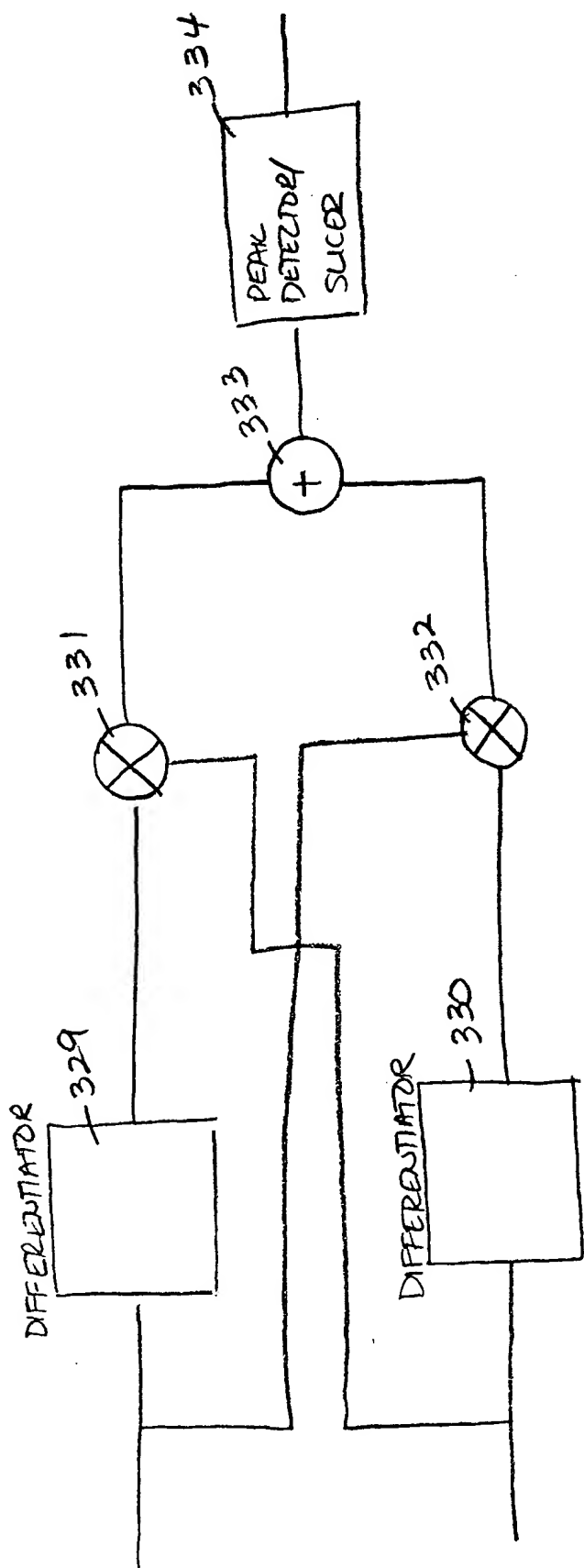


FIG. 21

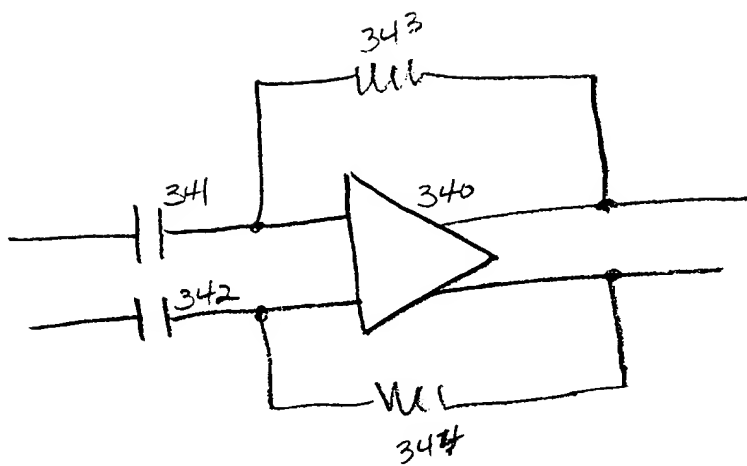


FIGURE 22

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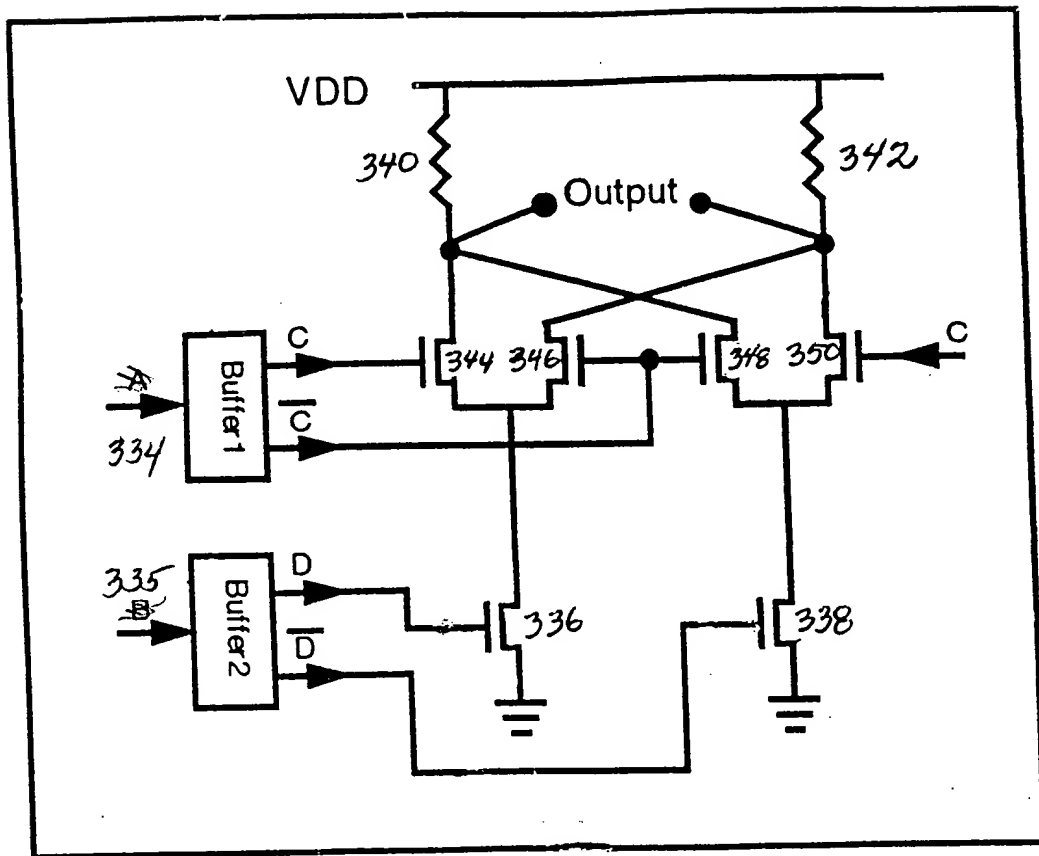


FIG. 23

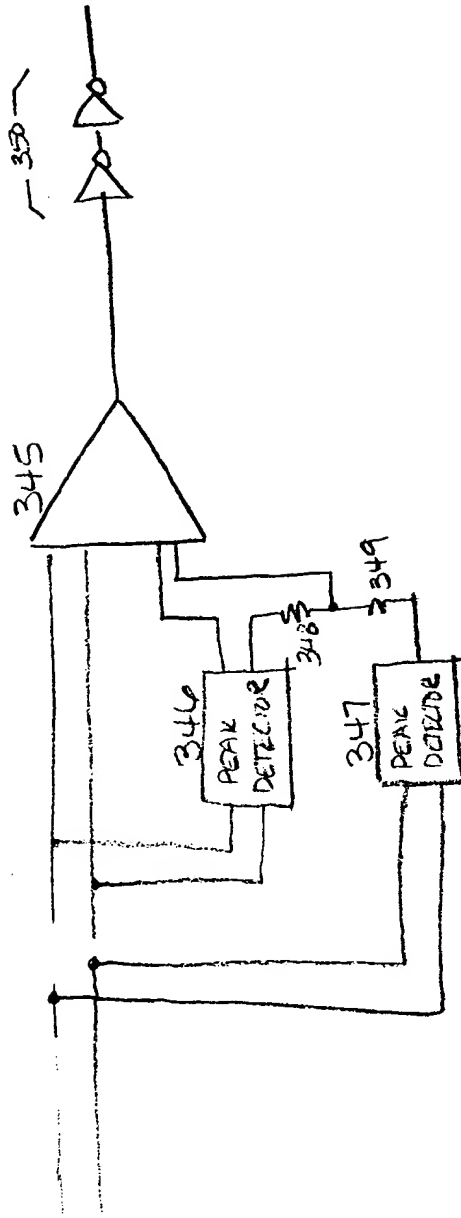


FIGURE 24



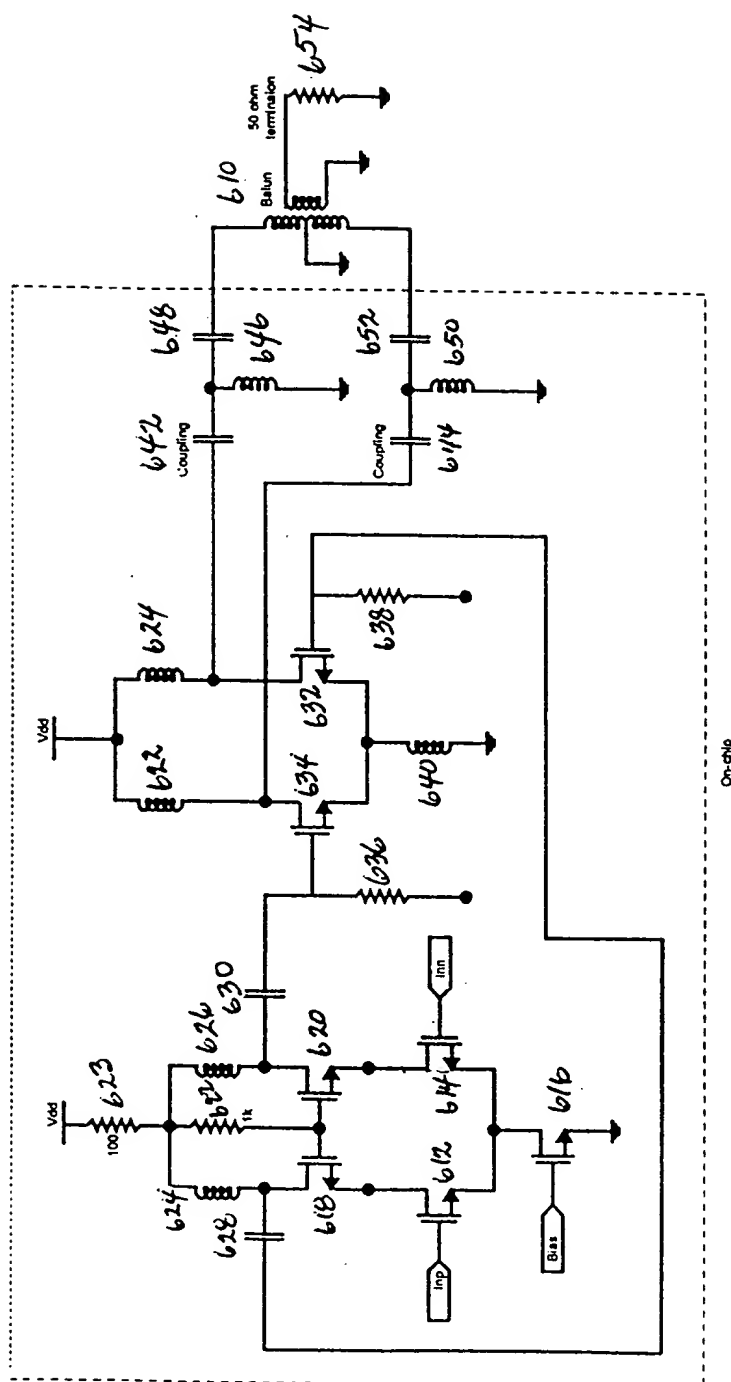


FIG. 25

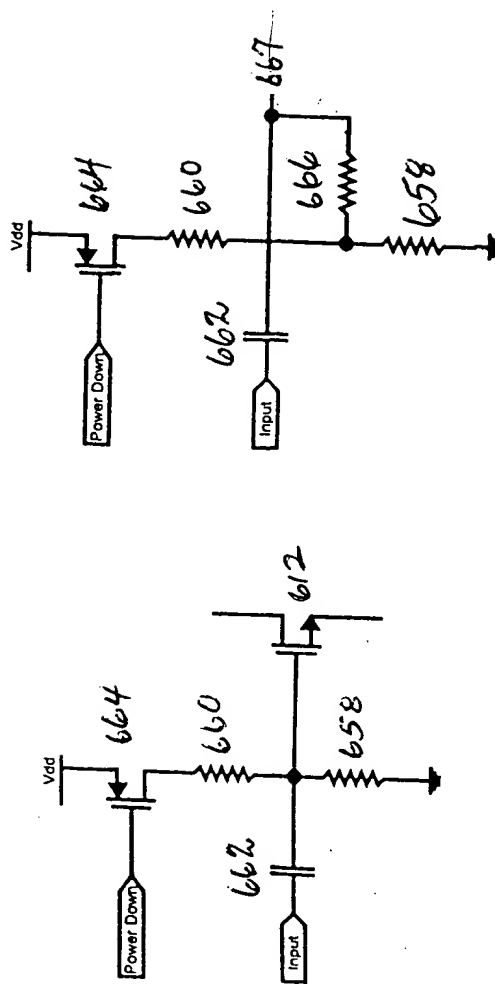


FIG. 26(b)

FIG. 26(a)

FIG. 27

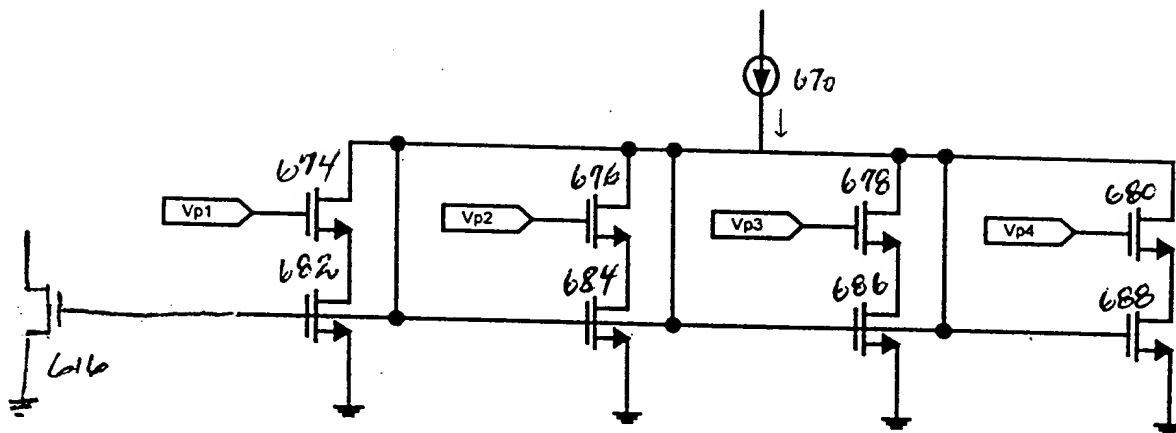


FIG. 28

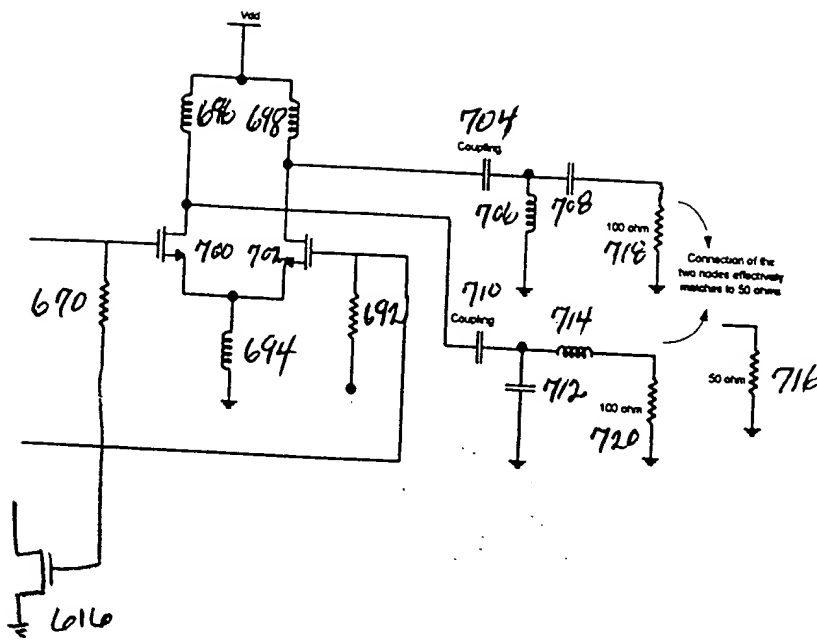


FIG. 29

FIG. 30

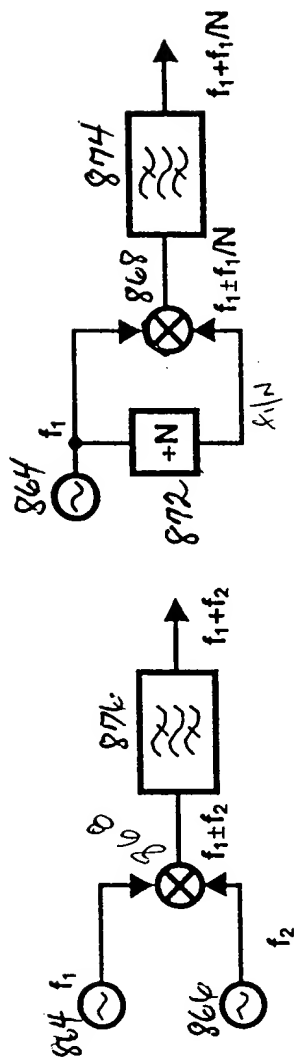


FIG. 31(a)

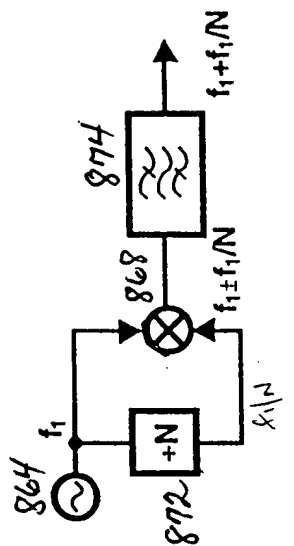


FIG. 31(b)

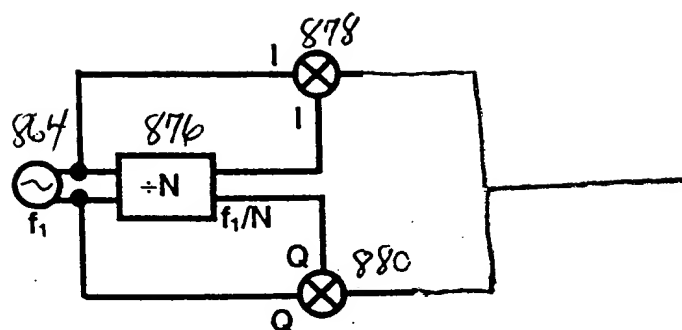


FIG. 32



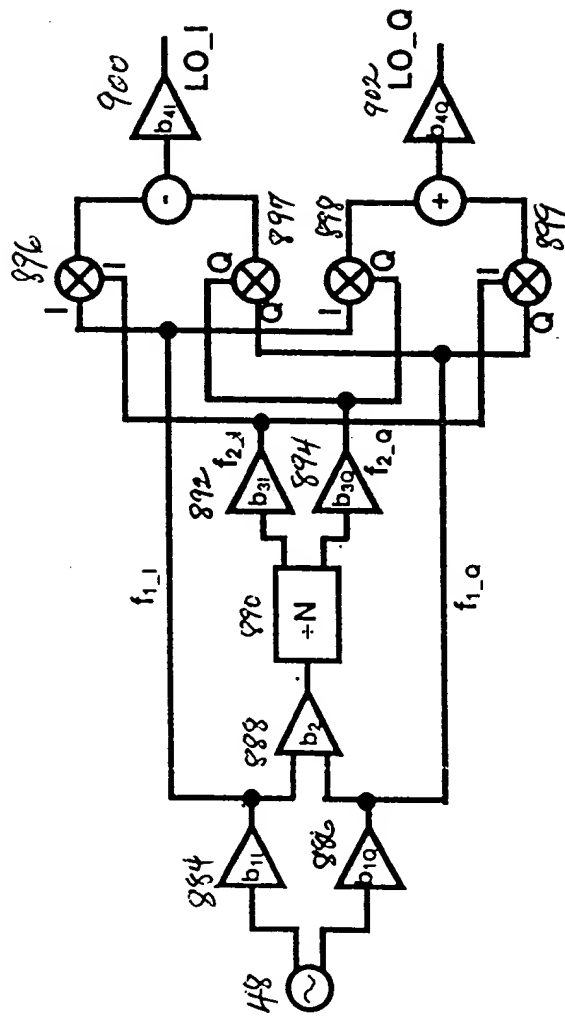


FIG. 33

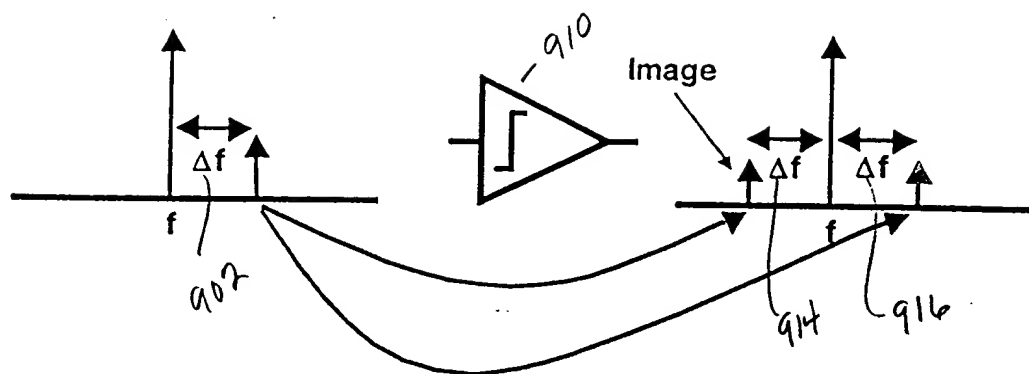


FIG. 33(a)

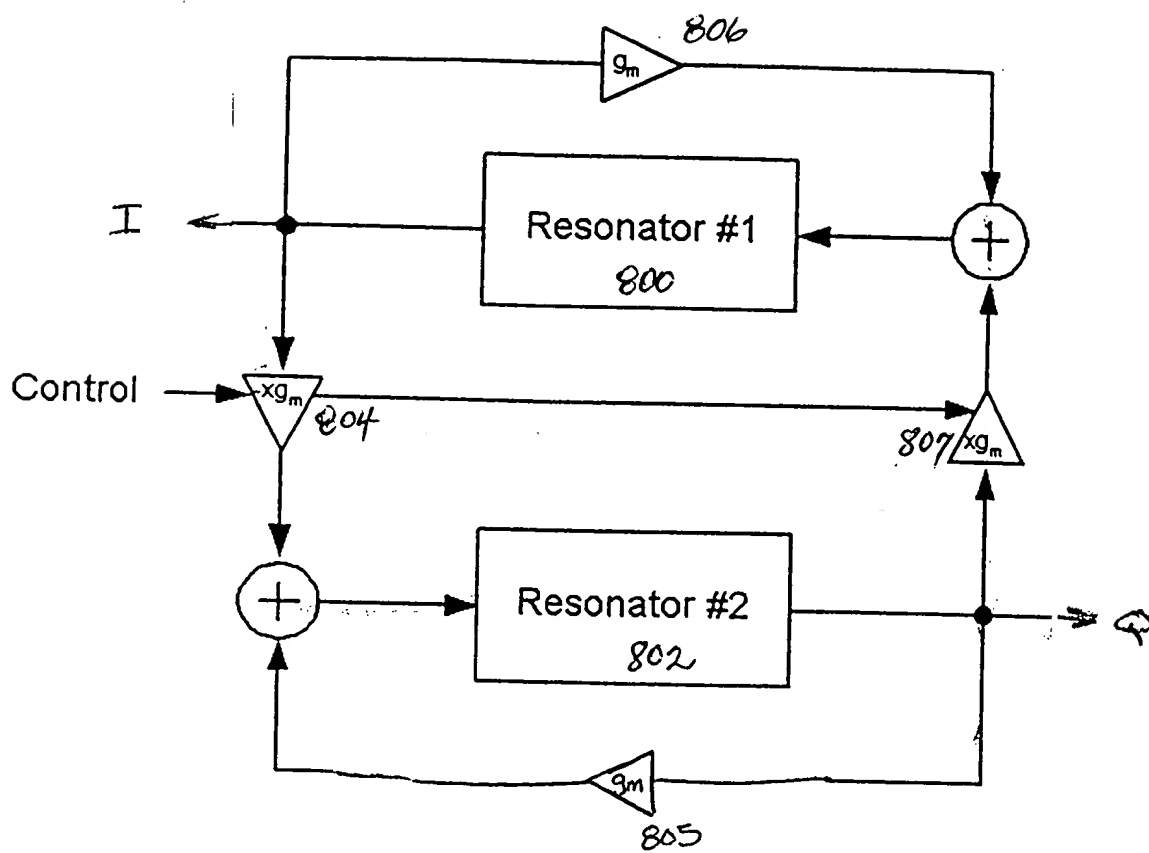


FIG. 34

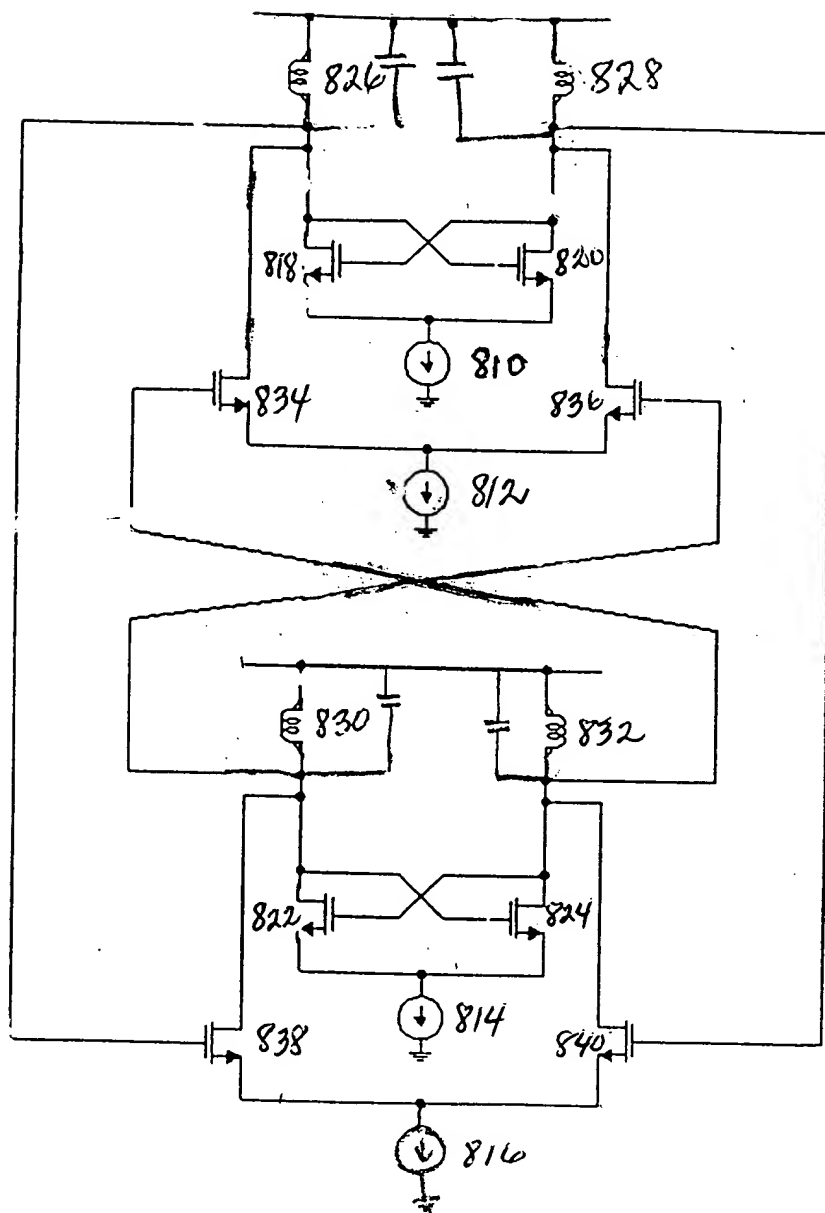


FIG. 35

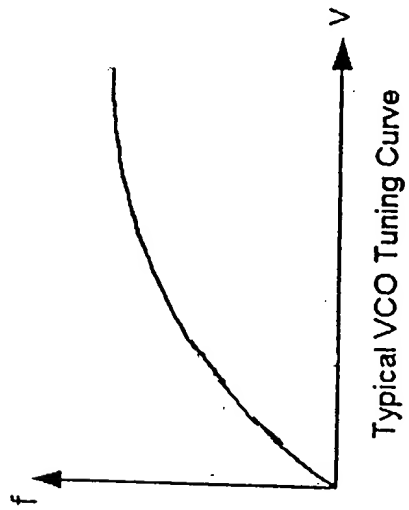


FIG. 36(a)

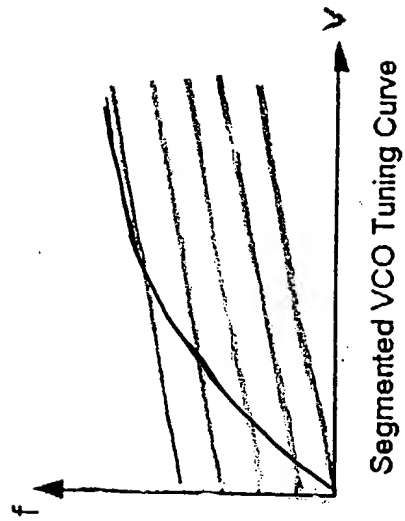


FIG. 36(b)

FIG. 37(a)

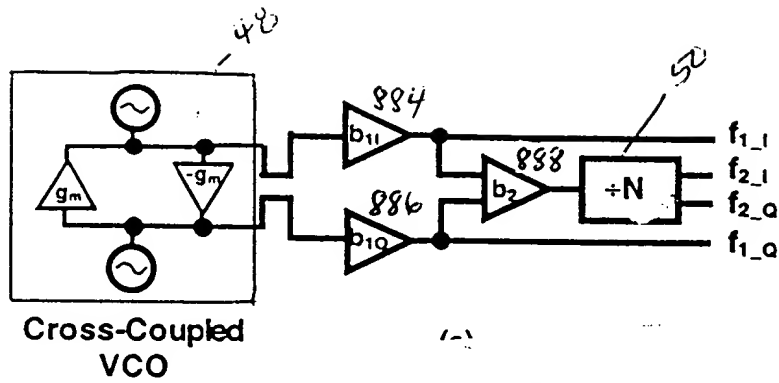
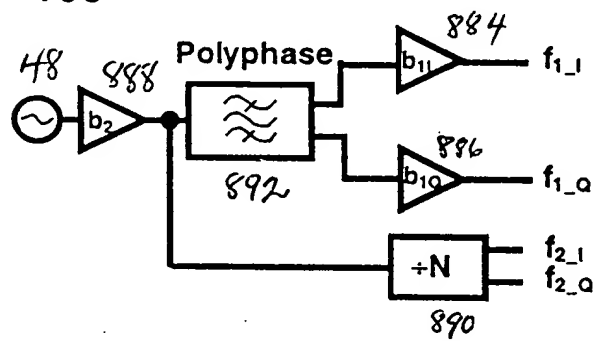


FIG. 37(b)





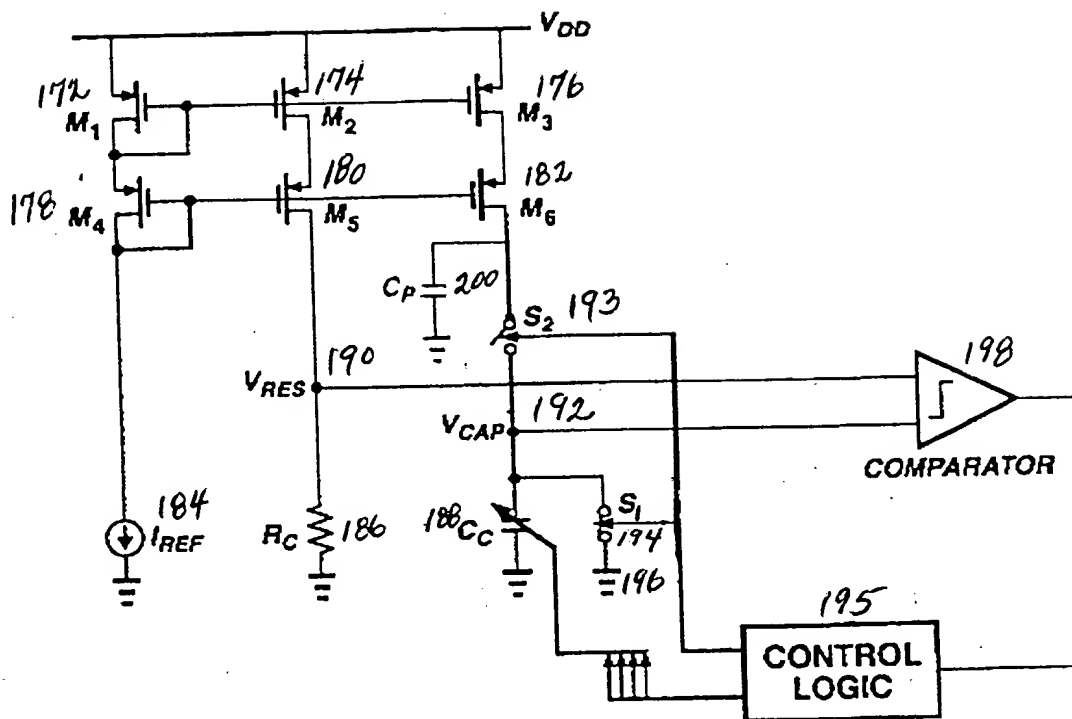


FIG. 39



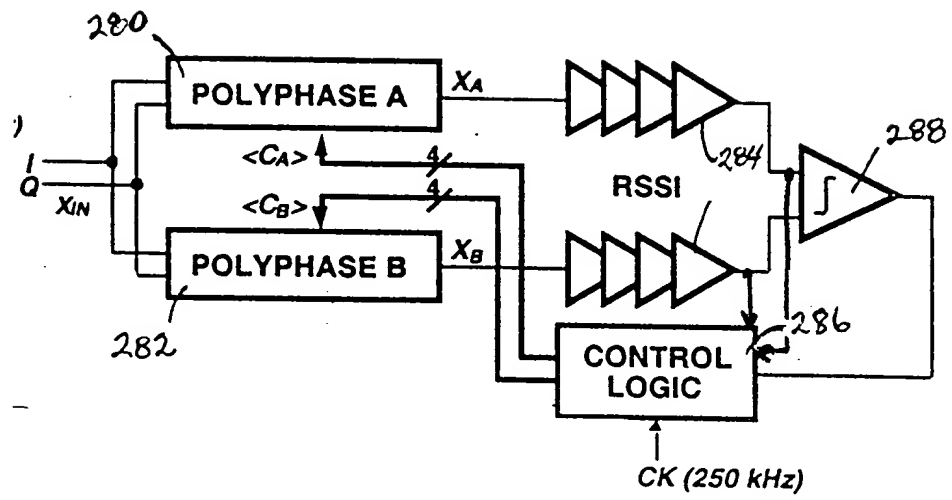


FIG. 40

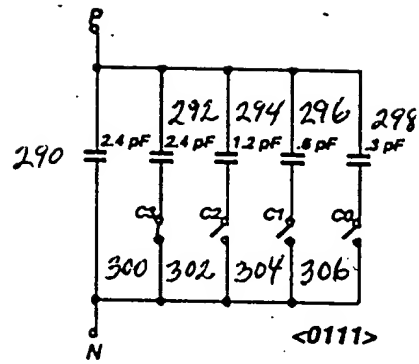


FIG. 41

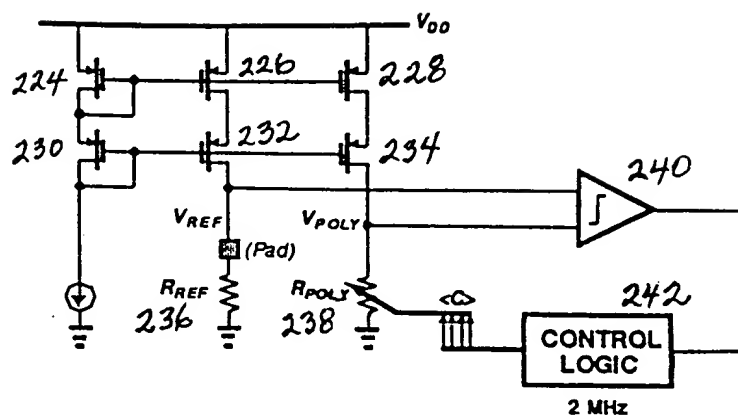


FIG. 42

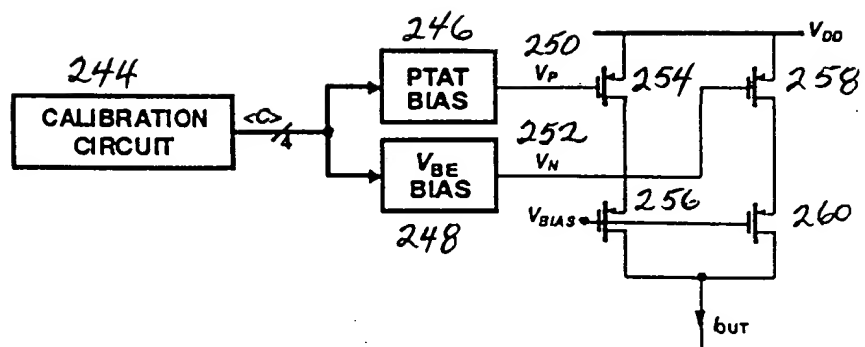
[illegible]

FIG. 43

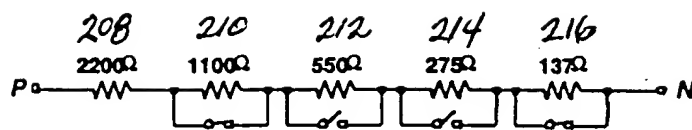


FIG. 44

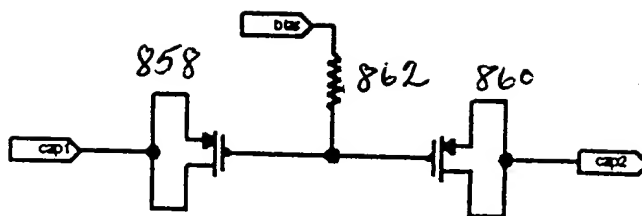
[illegible]

FIG. 45

642 644 646 648 650 652

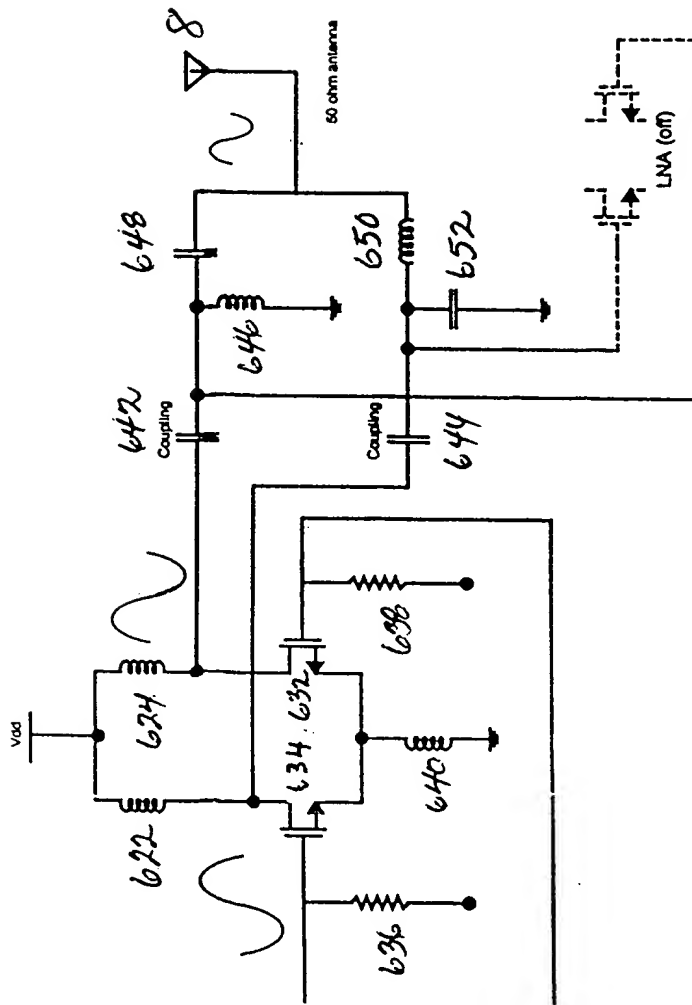


FIG. 46

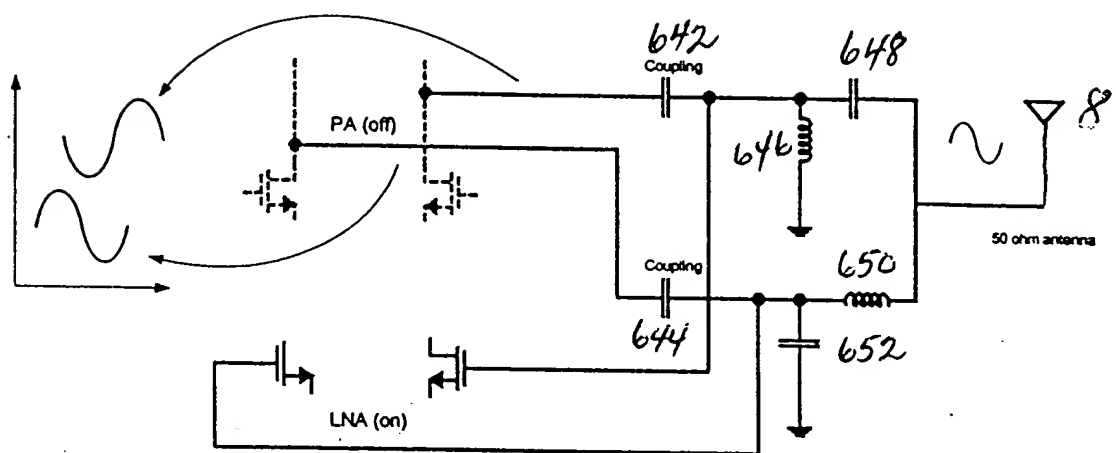


FIG. 47